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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,380	06/12/2006	Steven C. Deane	GB030221	5921
24737 7590 01/03/2008 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			EXAMINER NHU, DAVID	
			ART UNIT	PAPER NUMBER
			2818	
			MAIL DATE	DELIVERY MODE
			01/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/596,380

Applicant(s)

DEANE, STEVEN C.

Examiner

David Nhu

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 November 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

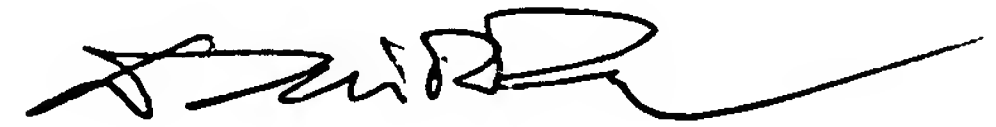
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTIONS

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 5-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Young (2006/0030084 A1).

Regarding claim 5, Takayama, (see figures 1-13, para 0033 to 0098), teaches an active matrix pixel device, comprising: a plurality of polycrystalline silicon islands TFT1, TFT2 supported by a substrate 100, one of the polycrystalline silicon islands providing a channel and doped source/drain regions s1, s2, d1, d2 of a thin film transistor, the active matrix pixel further comprising a PIN diode D, which includes a p-type doped region and an n-type doped region separated by an amorphous silicon intrinsic region 40, wherein the amorphous silicon intrinsic region overlies and contacts at least a part of one the polycrystalline silicon islands, which provides one of the p-type or n-type doped regions (see figures 1, 2, 13).

Regarding claims 6-11, Young, (see figures 1-13), teaches the doped source/drain regions and said one of the p-type or n-type doped regions of the PIN diode are provided by the same polycrystalline silicon island; both the p-type and n-type doped regions of the PIN diode are provided by respective of the polycrystalline silicon islands; a second thin film transistor having doped source/drain regions provided by one of the polycrystalline silicon islands, the doped source/drain regions being of an opposite conductivity type; wherein a

transparent conductive gate 19a overlies the intrinsic amorphous silicon region of the PIN diode separated by an insulating layer 15, the gate serving to apply a voltage to the amorphous silicon intrinsic region so as to control the conductivity between the n-type and p-type doped regions; the thin film transistor further comprises a gate electrode, which serves to control a current through the channel, and wherein the amorphous silicon intrinsic region of the PIN diode overlies the gate electrode; the PIN diode serves to measure a light intensity output from an associated display element and supply a signal to drive circuitry connected to enable modulation of the light intensity output.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Zhang'000 and Takayama'694 are cited as of interest.
4. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Nhu, (571)272-1792.

The examiner can normally be reached on Monday-Friday from 7:00 AM to 5:30 PM. *The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300. Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.*

Should you have questions on access to the Private PAIR system, contact the Electronic

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Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu 



December 21, 2007